AND 18 2004 STORES	IN THE UNITED STATES	PATE	NT AND TRAI	DEMARK OFFICE
TENT & TREE IN Re	the Application of:)		
	Anand S. Murthy et al.)	Art Unit:	2823
Serial	No.: 09/831,539)	Examiner:	Kebede, Brook
Filed:	April 15, 2002)		
For:	METHOD OF FABRICATING A FIELD))		
	EFFECT TRANSISTOR STRUCTURE)		
	WITH ABRUPT SOURCE/DRAIN)		
JUNCI	TIONS (AS AMENDED)			
Mail	Stop ISSUE FEE			
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INFORMATION DISCLOSURE STATEMENT

Sir:

Alexandria, VA 22313-1450

Enclosed is a copy of Information Disclosure Citation Form PTO-SB/08A together with copies of the documents cited on that form. It is respectfully requested that the cited documents be placed in the file. These references are cumulative to the references previously cited. This Information Disclosure Statement is being submitted pursuant to 37 C.F.R. §1.97(i).

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Mail Stop ISSUE FEE, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on August 10, 2004

(Date of Deposit)

Claire Wallters

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09/831,539 -1-

42390.P6624US Patent

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

The Commissioner is hereby authorized to charge any fees in connection with this communication to our Deposit Account No. 02-2666.

Respectfully submitted,

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Substitute f	or Form 1449/I	то	R. E		Complete	if Kn	own	
STATEMENT BY APPLICANT					Filing Date April 1:		831,539	
							11 15, 2002	
							and S. Murthy	
					Art Unit	1	2823	
					Examiner Name	 	oede, Brook	
Sheet	1		of 2		Attorney Docket Number		90.P6624US	
	<u> </u>		U.S. PATENT D	OCUMENTS				
Examiner Initials*	Cite No. ¹	Num	Document Number ber-Kind Code ² (If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Docun	nent	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US-	4,963,502	10-16-1990	Teng et al.			
		US-	5,949,116	09-07-1999	Wen			
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		US-	6,010,936	01-04-2000	Son		_	
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		US-	6,025,235	02-15-2000	Krivokapic			
		US-						
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Examiner Cite	Foreign Patent Document	Publication	Name of Patentee or	Pages, Columns, Lines,	T	
nitials*	No. ¹	Country Code ³ Number ⁴ Kind Code ⁵ (if known)	Date MM-DD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	

Examiner	Date Considered	
Signature		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. There Office that issued the document, by the two-letter code (WIPO Standard ST.3). For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known				
Application Number	09/831,539			
Filing Date	April 15, 2002			
First Named Inventor:	Anand S. Murthy			
Art Unit	2823			
Examiner Name	Kebede, Brook			
Attorney Docket Number	42300 P6624LIS			

Sheet	2	of 2	Attorney Docket Number	42390.P6624US	
		N	ON PATENT LITERATURE DOCUMENT	rs	
Examiner Initials*	Cite No ¹			-2	
			Silicon Processing For The VLSI Era, Volume nset Beach, CA 90742, U.S.A., pgs. 171-172,		
			-		

Examiner	Date Considered	•
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